AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method, comprising:

retrieving a first instruction from a memory unit via an n-bit input path;

pre-decoding the first instruction at a direct memory access unit;

providing the pre-decoded first instruction from the direct memory access unit to a processing element via a q-bit output path, where $n < q$;

decoding the pre-decoded first instruction at the processing element;

executing the completely decoded instruction at the processing element;

determining, based on said executing, that a second instruction subsequent to the first instruction will not be executed; and

arranging for a pre-decoded second instruction to not be provided from the direct memory access unit to the processing element.

2. (Previously Presented) The method of claim 1, wherein said providing comprises storing the pre-decoded first instruction in memory local to the processing element.

3-4. (Canceled)

5. (Original) The method of claim 1, further comprising:

loading instructions into the memory unit during a boot-up process.

6. (Original) The method of claim 1, wherein the processing element is a reduced instruction set computer device.

7. (Previously Presented) The method of claim 6, wherein the pre-decoded first instruction comprises execution control signals.

8. (Previously Presented) An apparatus, comprising:

an n-bit input path to receive a first instruction from a memory unit;

a direct memory access unit including an instruction pre-decoder to pre-decode the received first instruction;

a q-bit output path to provide a pre-decoded first instruction from the direct memory access unit, where $n < q$; and

a processor to (i) receive the pre-decoded first instruction from the q-bit output path, (ii) decode the pre-decoded first instruction, (iii) determine that a second instruction, subsequent to the first instruction, will not be executed, and (iv) arrange for a pre-decoded second instruction not be provided from the direct memory access unit to the processor.

9. (Original) The apparatus of claim 8, further comprising:

the memory unit coupled to the input path.

10. (Canceled)

11. (Previously Presented) The apparatus of claim 8, wherein the processing element includes a local memory to store the pre-decoded first instruction.

12. (Previously Presented) The apparatus of claim 8, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder.

13. (Canceled)

14. (Previously Presented) The apparatus of claim 8, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit.

15. (Previously Presented) The apparatus of claim 8, wherein the processing element is a reduced instruction set computer device having an instruction pipeline.

16. (Previously Presented) An article, comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a machine result in the following:

retrieving a first instruction from a memory unit via an n-bit input path,

pre-decoding the first instruction at a direct memory access unit,

providing via a q-bit output path the pre-decoded first instruction from the direct memory access unit to a processing element to be decoded, where $n < q$,

retrieving a second instruction, subsequent to the first instruction, from the memory unit,

pre-decoding the second instruction at the direct memory access unit,

receiving from the processing element an indication that the second instruction will not be executed, and

deleting the pre-decoded second instruction without providing the pre-decoded second instruction from the direct memory access unit to the processing element.

17. (Previously Presented) The article of claim 16, wherein said providing comprises storing the pre-decoded first instruction in memory local to the processing element.

18-20. (Canceled)

21. (Currently Amended) A system, comprising:

a multi-directional antenna;

an apparatus having a direct memory access unit that includes:

an n-bit input path to receive a first instruction from a memory unit,

an instruction pre-decoder to pre-decode the first instruction, and

a q-bit output path to provide a pre-decoded first instruction, where $n < q$, wherein the direct memory access unit is further to receive and pre-decode a second instruction without sending the pre-decoded second instruction via the output path; and

a processor to receive and decode the pre-decoded first instruction received via the q-bit output path.

22. (Original) The system of claim 21, wherein the apparatus is a digital base band processor.

23. (Original) The system of claim 22, wherein the digital base band processor is formed as a system on a chip.

24. (Original) The system of claim 21, wherein the system is a code-division multiple access base station.